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On July 25, 2001

TOWNSEND and TOWNSEND and CREW LLP

By: _____

PATENT
000939-085400US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Byoung Kwon Cha

Application No.: Unassigned

Filed: Herewith

For: PROGRAM CIRCUIT

Examiner: Unassigned

Art Unit: Unassigned

REISSUE APPLICATION
PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination of the above-referenced application, please enter the following amendments and remarks.

IN THE CLAIMS:

Please add new claims 5-49 as follows:

Claim 5. The program circuit as claimed in claim 1, wherein said comparator includes eight exclusive-NOR gates to compare the output data of said data input buffer and the output data of said sense amplifier.

Claim 6. A non-volatile memory device, comprising:

a plurality of memory cells;

an input component coupled to the memory cells and configured to transmit first information to the memory cells, the first information being N bits of data; and

a primary circuit configured to transmit second information to the memory cells if the primary circuit determines that the first information has not been properly inputted into the memory cells, the second information being M bits of data, where M is less than N.

Claim 7. The non-volatile memory device of claim 6, wherein the primary circuit includes:

a detecting circuit to determine whether the first information has been properly inputted into the memory cells.

Claim 8. The non-volatile memory device of claim 7, wherein the detecting circuit compares the first information in the input component and information read from the memory cells to determine whether the first information has been properly inputted into the memory cells.

Claim 9. The non-volatile memory device of claim 6, wherein the second information is information inputted to memory cells selected from the memory cells that have been inputted with the first information.

Claim 10. The non-volatile memory device of claim 9, wherein the second information is transmitted only to the memory cells for which data have not been properly written.

Claim 11. The non-volatile memory device of claim 10, wherein N is 8 or 4.

Claim 12. The non-volatile memory device of claim 11, wherein M is two or less.

Claim 13. The non-volatile memory device of claim 6, wherein N is one selected from the group consisting of: 32, 16, 8, 4, and 2.

Claim 14. The non-volatile memory device of claim 6, wherein the first information is transmitted to perform a program operation.

Claim 15. The non-volatile memory device of claim 6, wherein the first information is transmitted to perform an erase operation.

Claim 16. A non-volatile memory device, comprising:

a plurality of memory cells;

an input component coupled to the memory cells and configured to program first information into the memory cells; and

a primary circuit configured to reprogram only the memory cells that have not been properly programmed.

Claim 17. The non-volatile memory device of claim 16, the primary circuit including:

a first circuit to determine if the first information has been properly programmed into the memory cells; and

a second circuit to transmit a signal to initiate reprogramming of any memory cells that has not been properly programmed.

Claim 18. The non-volatile memory device of claim 16, wherein the first information is no more than four bits of data and are programmed in parallel.

Claim 19. The non-volatile memory device of claim 16, wherein the first information is no more than two bits of data and are programmed in parallel.

Claim 20. A semiconductor device, comprising:

a plurality of memory cells;

an input component coupled to the memory cells and configured to program the memory cells;

a comparator to determine whether first information of the input component has been properly programmed into the memory cells, the comparator having a logic gate to output a first signal to indicate whether or not a reprogramming operation is needed, wherein the first information is N bits of data; and

a controller coupled to the comparator and configured to output a second signal to initiate reprogramming of M number of the memory cells, where M is less than N.

Claim 21. The device of claim 20, wherein the comparator compares the first information of the input component with second information read from the memory cells.

Claim 22. The device of claim 21, wherein N is eight and the input component is configured to transmit a byte of information at a time to the memory cells.

Claim 23. The device of claim 22, wherein the comparator includes:

a plurality of XNOR gates having first and second input ports, the first input ports being configured to receive the first information and the second input ports being configured to receive the second information, wherein outputs of the XNOR gates indicate whether the first information and the second information are the same.

Claim 24. The device of claim 23, wherein the comparator includes N number of the XNOR gates.

Claim 25. The device of claim 23, wherein the comparator further includes:

a logic gate coupled to the outputs of the XNOR gates, the logic gate configured to output the second signal.

Claim 26. The device of claim 23, further comprising:

a sense amplifier coupled to the memory cells, wherein the sense amplifier provides the second information to the second input ports of the XNOR gates.

Claim 27. The device of claim 26, further comprising:

a latch configured to receive information relating to the first information of the input component.

Claim 28. The device of claim 27, wherein the latch receives the outputs of the XNOR gates.

Claim 29. The device of claim 28, wherein the latch includes N number of flip-flops to receive the outputs of the XNOR gates.

Claim 30. The device of claim 27, wherein the information received by the latch is the first information of the input component.

Claim 31. The device of claim 27, wherein an output of the latch is transmitted to the controller.

Claim 32. The device of claim 31, wherein the first information of the input component is transmitted to the controller.

Claim 33. The device of claim 32, wherein the first information and the output of the latch are eight bits of data, respectively, where the controller outputs eight signals in response to receipt of the first information and the output of the latch, the eight signals having one or more signals of first type to initiate reprogramming of corresponding one or more memory cells that have not been properly programmed and one or more of signals of second type to disable reprogramming of corresponding one or more memory cells that have been properly programmed.

Claim 34. The device of claim 20, wherein N is 2.

Claim 35. The device of claim 20, wherein N is one selected from one of the following: 32, 16 and 8.

Claim 36. The device of claim 20, wherein M corresponds to a number of the memory cells that have not been properly programmed.

Claim 37. The device of claim 36, wherein M is proportional to the number of the memory cells that have not been properly programmed.

Claim 38. The device of claim 36, wherein M is equal to the number of the memory cells that have not been properly programmed.

Claim 39. The device of claim 20, wherein N is 4.

Claim 40. The device of claim 39, wherein M is 2.

Claim 41. A non-volatile semiconductor device, comprising:

a plurality of memory cells;

a sense amplifier coupled to the memory cells to read information written into the memory cells;

an input data buffer coupled to the memory cells and configured to transmit N bits of information at a time into the memory cells;

a comparator having a plurality of logic gates to compare bit-by-bit first information of the input data buffer with second information of the sense amplifier and output a reprogram operation signal if the first information and the second information are different;

a data latch circuit coupled to outputs of one or more of the logic gates of the comparator; and

a controller having a plurality of logic gates and being configured to receive the first information of the input data buffer and outputs of the data latch circuit, and output a signal for applying a program bias voltage to any memory cell that has not been properly programmed.

Claim 42. The non-volatile device of claim 41, wherein the plurality of logic gates of the controller include a first set of logic gates of N numbers corresponding to the N bits of information programmed into the memory cells, the first set of logic gates being configured to output a high voltage signal for any bit of information that has not been properly programmed into the memory cells.

Claim 43. The non-volatile device of claim 42, wherein the signal for applying the program bias voltage is a low voltage signal.

Claim 44. A non-volatile semiconductor device, comprising:

a plurality of memory cells;

a sense amplifier coupled to the memory cells;

an input data buffer coupled to the memory cells and configured to write N bits of information at a time into the memory cells;

a comparator having N number of XNOR gates corresponding to the N bits of information being written into the memory cells, the comparator being configured to compare bit-by-bit N bits of first information of the input data buffer with N bits of second information of the sense amplifier and output a rewrite operation signal if any bit of the first information and the second information is different from each other;

a data latch circuit coupled to the comparator to receive outputs of the XNOR gates; and

a controller having a plurality of logic gates and being configured to receive the first information of the input data buffer and outputs of the data latch circuit, and configured to output a signal for applying a bias voltage to any memory cell that has not been properly written,

wherein the plurality of logic gates of the controller include a first set of logic gates of N numbers corresponding to the N bits of information written into the memory cells, the first set of logic gates being configured to output a high voltage signal for any bit of information that has not been properly written into the memory cells.

Claim 45. A non-volatile memory device, comprising:

a plurality of memory cells;

an input component coupled to the memory cells and configured to write information into the memory cells; and

a circuit configured to rewrite only the memory cells that have not been properly written.

Claim 46. The non-volatile memory device of claim 45, wherein the information is one bit of information, the device being configured to write one bit of information at a time.

Claim 47. A method of operating a non-volatile semiconductor memory device having a plurality of memory cells, the method comprising:

writing information into N number of the memory cells;

determining if the information has been properly written into the memory cells; and

rewriting at least a portion of the information to M number of the memory cells if any bit of the information has not been properly written into any of the N number of the memory cells, wherein M is less than N.

Claim 48. The method of claim 47, wherein the determining step involves checking each of the N memory cells in a bit-by-bit comparison.

Claim 49. The method of claim 47, wherein the writing step involves programming the N number of the memory cells.

REMARKS

Claims 1-49 are pending in this reissue application. The written description has been amended to insert a priority claim to the reissue application. New claims 5-49 have been added. Support for the new claims is found in the specification. No new matter has been added.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

Steve Y. Cho
Reg. No. 44,612

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: (415) 576-0200
Fax: (415) 576-0300
SYC:asb
PA 3159260 v1